**Memory Elements**

Table of Contents

[General Memory Architecture 3](#_Toc64670443)

[Read Only Memory 4](#_Toc64670444)

[SRAM Basics 5](#_Toc64670445)

[Circuitry 5](#_Toc64670446)

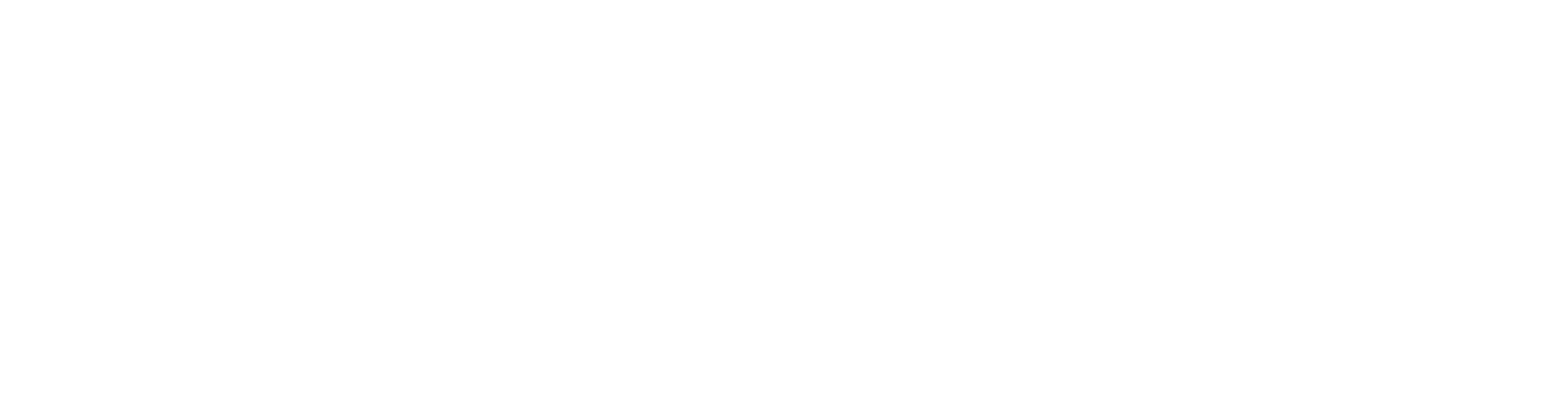
[6T SRAM Cell 6](#_Toc64670447)

[DRAM 8](#_Toc64670448)

[Operation 8](#_Toc64670449)

[Comparing Memory Types 9](#_Toc64670450)

Combinational circuits are incapable of remembering data on their own. To remember data, we need output values to be processed and given back as inputs somehow. Essentially, we need feedback.

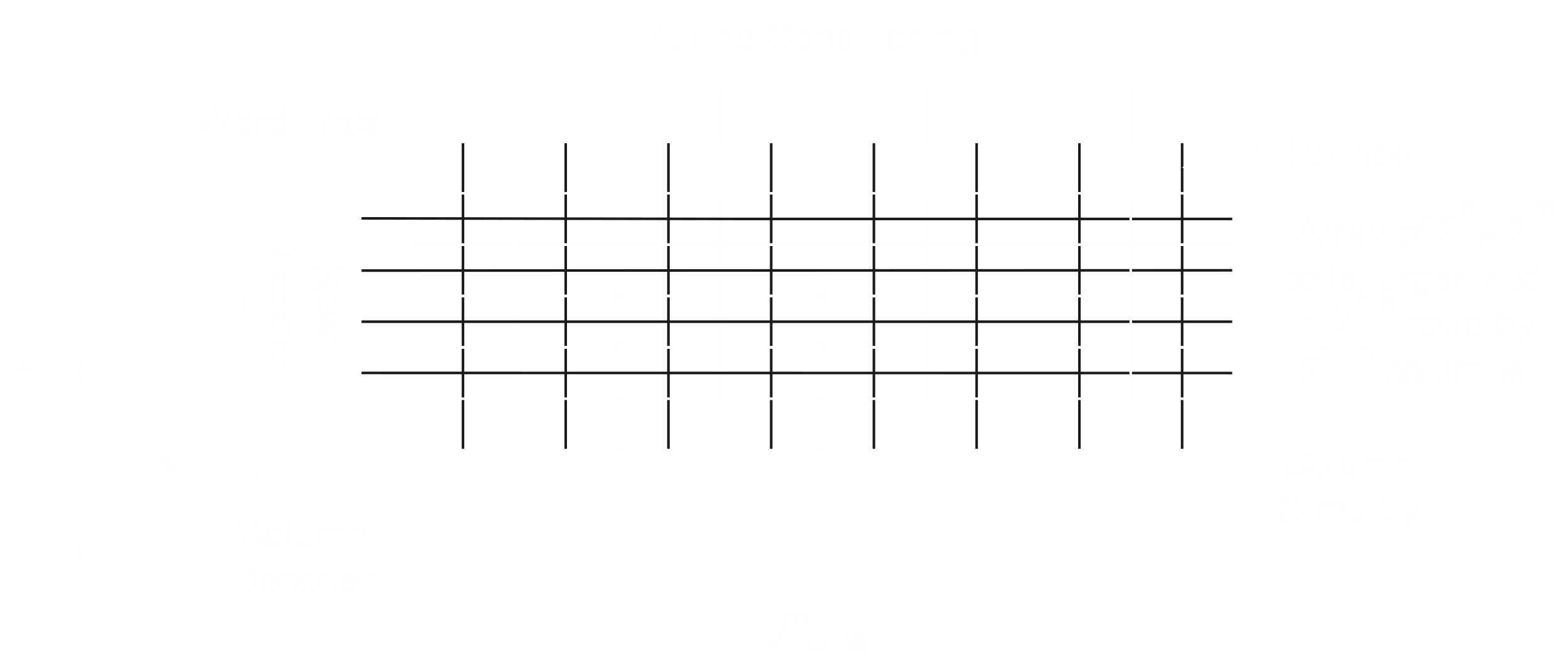


There are two types of memory elements:

1. Latches – These are level-sensitive, meaning the output depends on the level of the input.
2. Flip-Flops – These are edge-sensitive, meaning the output depends on the change from one level to another, whether the change is from a negative level to a positive level (positive edge sensitive) or from a positive level to a negative level (negative edge sensitive). In this sense, flip-flops are more sensitive than latches.

## General Memory Architecture

Memory is generally arranged as a 2D grid.



We can have words (rows), each of bits (columns). Generally, , which results in a tall structure. To deal with this, the array is folded so that each row contains words instead of . This means each row has bits.

Say we have words with bits per word. We want to arrange this into lines and columns. Thus, , and .

Large memories are built from smaller subarrays like this to maintain short word and bit lines. To access a particular cell, we need to activate the word line and the bit line for that cell.

## Read Only Memory

Read Only Memory (ROM) is a type of memory that permanently stores data on PCs and other electronic devices. In PCs, it holds the code needed to start a PC as well as major IO tasks and program and software instructions.

Since ROM is read only, it cannot be changed. It is permanent and non-volatile, meaning its memory is not lost when power is removed. This is in contrast to Random Access Memory (RAM), which is volatile.

There are numerous ROM chips located on the motherboard and a few on expansion boards as well. These are essential for the Basic Input/Output System (BIOS), boot process, reading and writing to peripheral devices, basic data management and the software for basic processes for certain utilities.

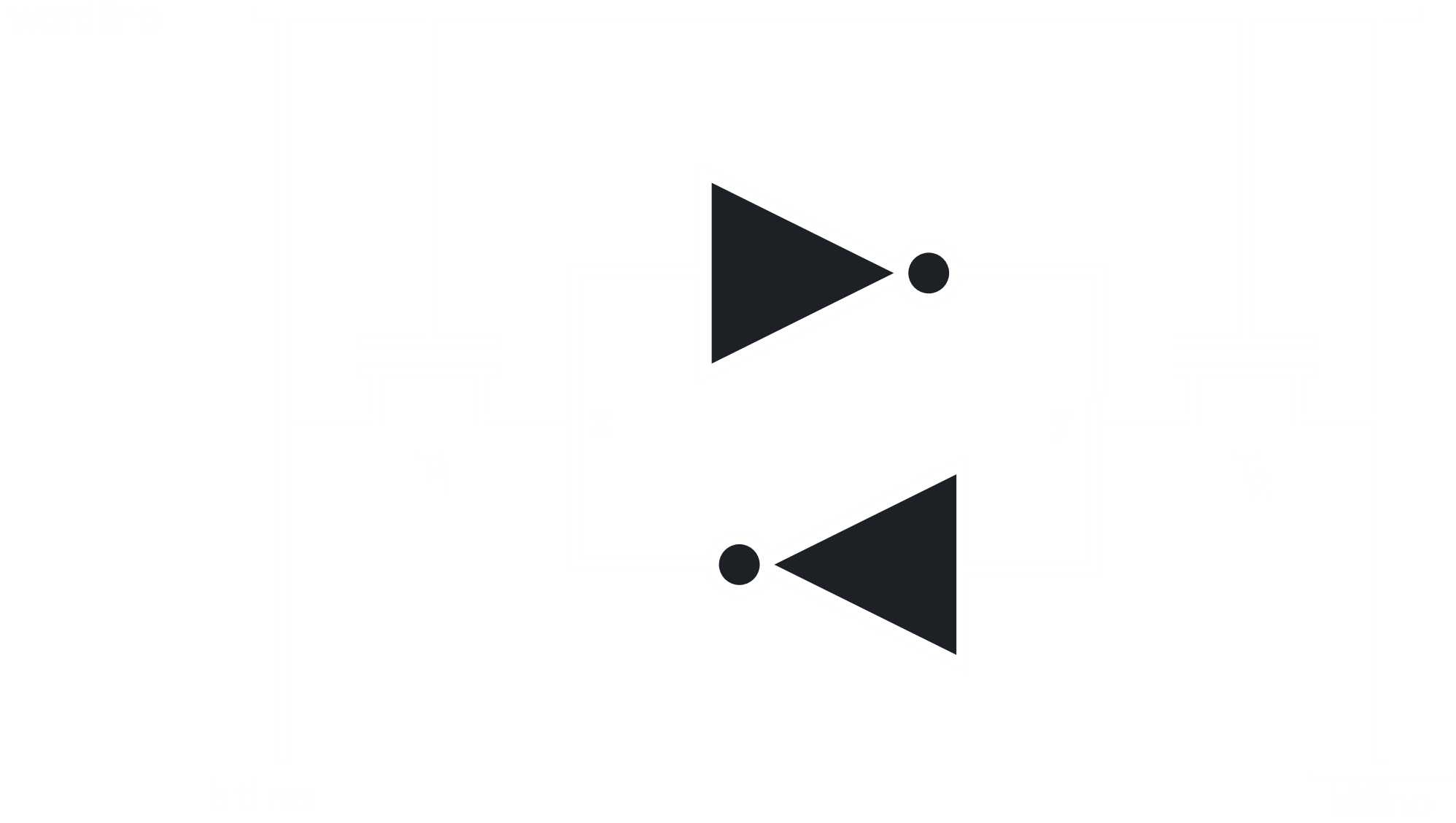
## SRAM Basics

Static Random-Access Memory (SRAM) is a form of semiconductor memory widely used in electronics, microprocessors and general computing applications. The data in SRAM is held in a static fashion and does not need to be dynamically updated, as is done in DRAM (which we will see next). However, the memory in SRAM is still volatile.

There are two key distinguishing features of SRAM:

* The data is held statically, meaning the data in the semiconductor memory will not need to be refreshed as long as power is available.
* It is a form of random-access memory, meaning we can read or write from anywhere in the memory in any order.

### Circuitry

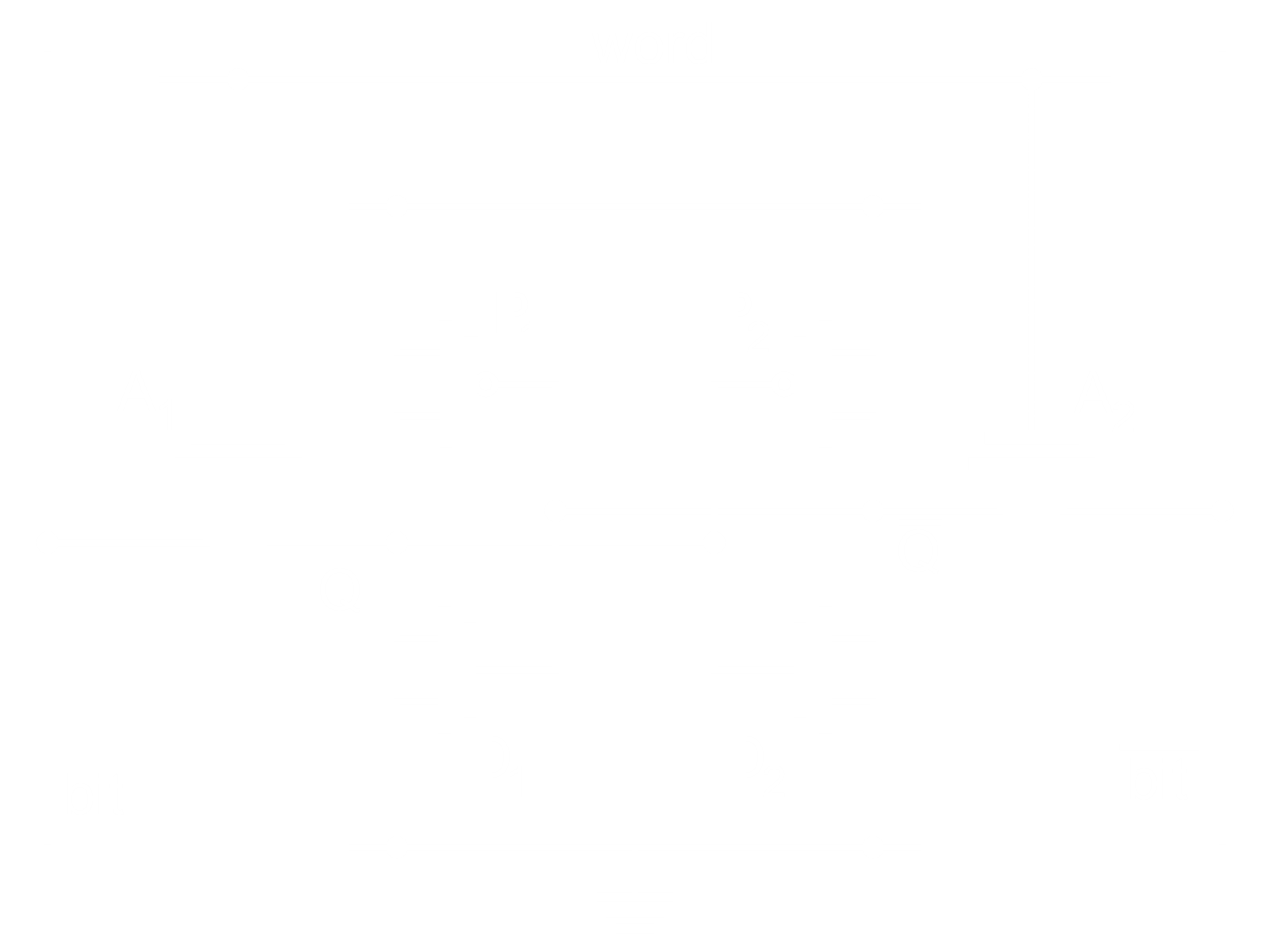


Two inverters are cross-connected to form a latch. The latch is connected to two bit lines with transistors and . The word line controls whether or not and are open. When the word line is in the ground level, the transistors are turned off and the latch retains its state.

During the read operation, the word line is activated to close the switches and . If the cell is in state , the signal on (on the left) is high and the signal on (on the right) is low. If the cell is in state , the opposite is true. The sense/write circuit at the end of the two bit lines monitor their state and set the corresponding outputs accordingly.

During the write operation, the sense/write circuit drives the bit lines and with the appropriate values and then activates the word line. This causes the cell to go into the required state, which the cell retains once the word line is deactivated.

### 6T SRAM Cell



In a 6T SRAM cell, the two inverters we saw in a basic SRAM are broken down into their transistor components. Hence, we have six transistors here.

The operation remains basically the same. During the read operation, the two bit lines are given some voltage. If is high, then the voltage from and are similar, so there is no discharge, but would be low, which would mean there is a difference in voltage between and . There will be a current flow along . Both bit lines are connected to a sense amplifier, which compares and . When is sensed to be higher than , an output of is given.

For a write operation, if we want to write onto the cell, is connected to the ground so that there is a voltage difference between and .

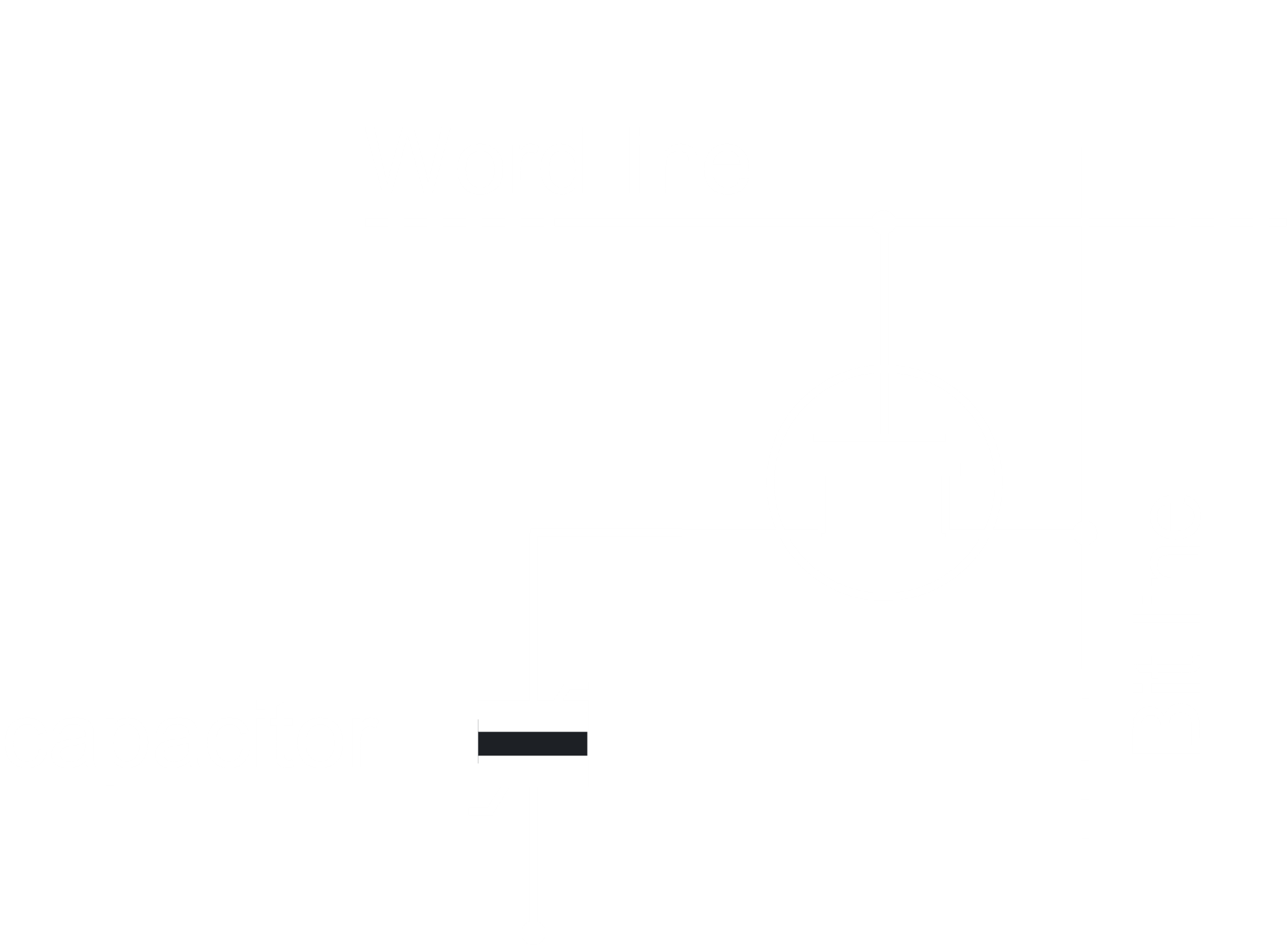
In either case, the word line must be activated to do anything.

## DRAM

Dynamic Random-Access Memory (DRAM) is generally used for data or program code that a computer processor needs to function. DRAM is commonly used in PCs, workstations and servers. Again, any part of the memory can be accessed in any order. DRAM is located close to a computer’s processor to allow faster access to data than would be available with hard disks or SSDs.

### Operation

DRAM stores each bit of data in a storage cell consisting of a capacitor and a transistor. Typically, a rectangular configuration of many such cells is used.



Before either the read or write operation, the word line must be activated to switch on the transistor. This allows access to the capacitor.

During the write operation, a voltage is applied to the bit line. This voltage is transferred to the capacitor and stored. However, capacitors have a tendency to discharge by themselves, so every once in a white, it has to be refreshed to maintain the bit. During the read operation, the bit line is not given a voltage. Instead, the charge from the capacitor is allowed to flow into the bit line, which is sensed. Sense amplifiers compare the capacitor voltage to a reference voltage to determine if the logic is . After reading, the capacitor must be restored to its original state by recharging it.

## Comparing Memory Types

|  |  |  |  |
| --- | --- | --- | --- |
| **Memory Type** | **SRAM** | **DRAM** | **Flash** |
| **Speed** | Very Fast | Fast | Very Slow |
| **Density** | Low | High | Very High |
| **Endurance** | Better | Better | Poor |
| **Power** | Low | High | Very Low |
| **Refresh** | No | Yes | No |
| **Retention** | Volatile | Volatile | Non-volatile |
| **Scalable** | Good | Bad | Good |
| **Mechanism** | Bi-stable latch | Capacitor | FN-tunnelling HCI |

DRAM is less scalable than the alternatives due to the use of capacitors, which are very large.